Cadence Full Custom IC Design

한국대학교 전자공학과
김길동

Content

1. Introduction

2. Digital Circuit
   - Logic Gate , MUX , Adder

3. Analog Circuit
   - CS · DIFF AMP

1. Introduction

Tools

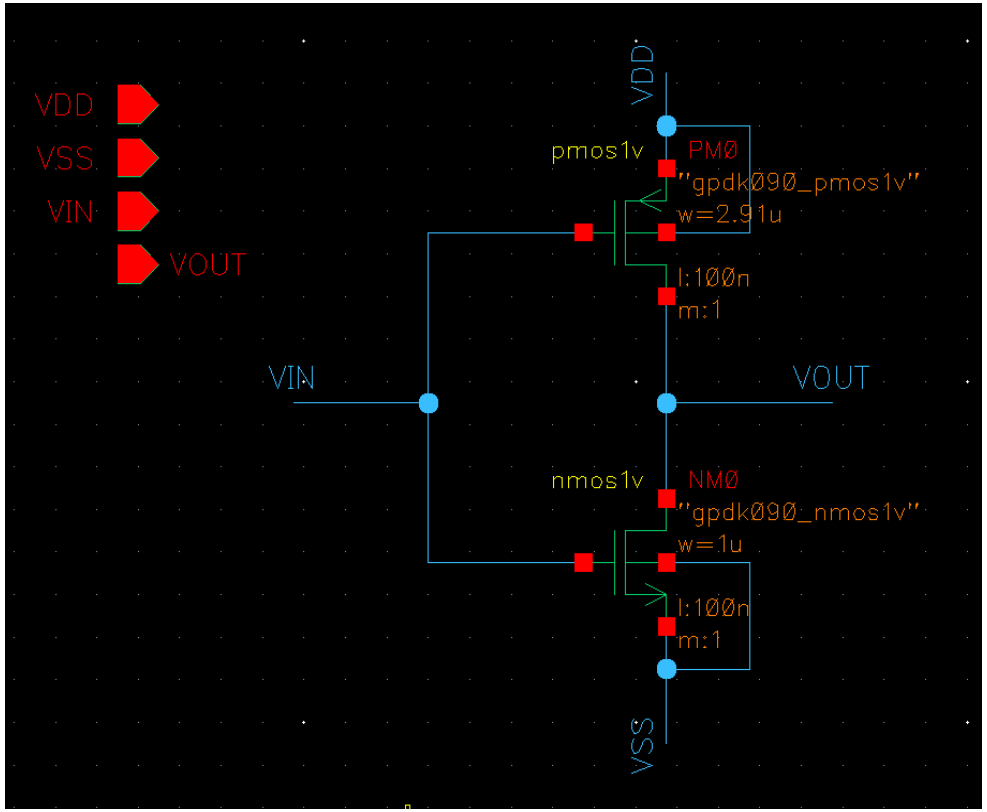
- Cadence Virtuoso Schematic Editor / Layout Editor
- Cadence Virtuoso Spectre/ADE
- Assura (DRC / LVS)
- GPDK090_v4.6

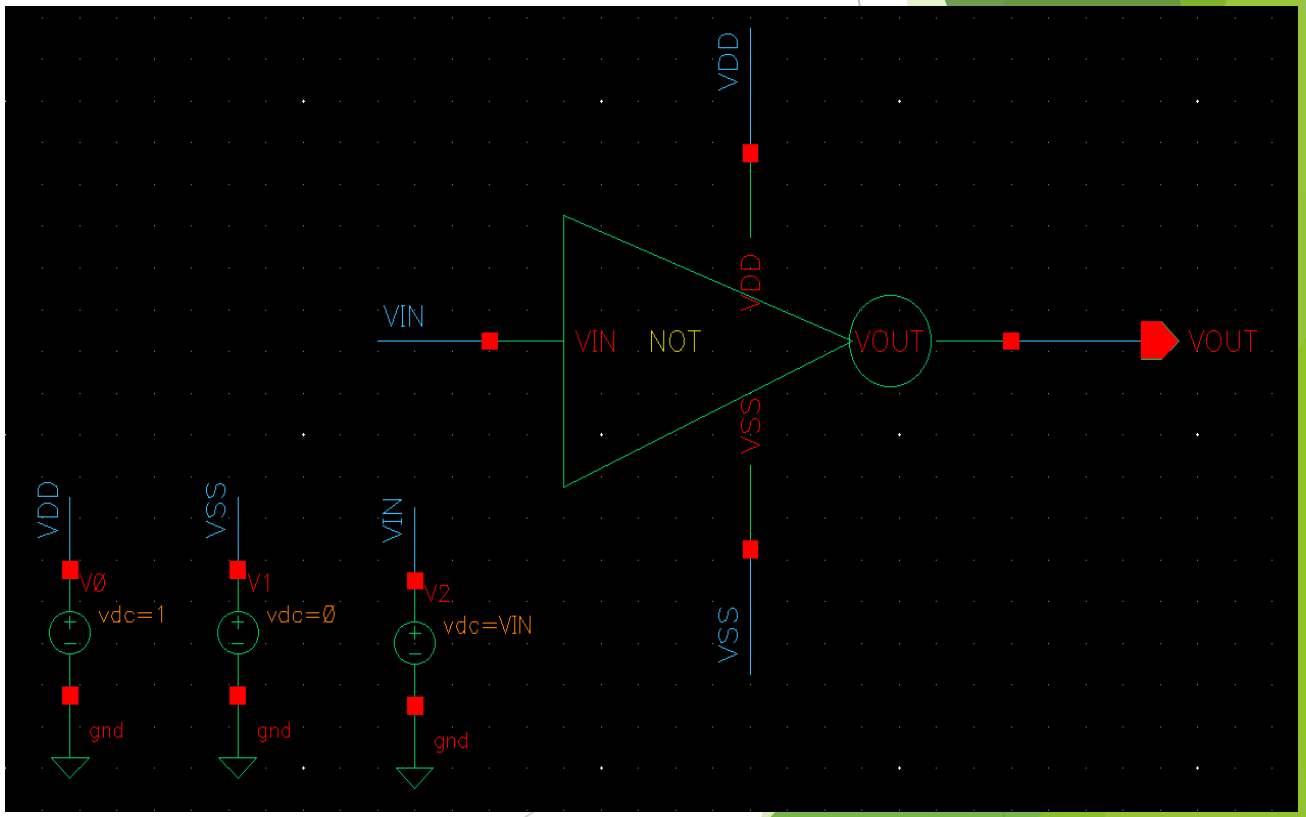
2. Digital Circuit

Digital Circuit	Logic Gate	Inverter 2NAND, 2NOR 3NAND, 3NOR Switch
	Multiplexer	2x1 MUX (Logic & Switch) 4x1 MUX (Logic & Switch)
	Adder	Half Adder Full Adder 4-bit Adder

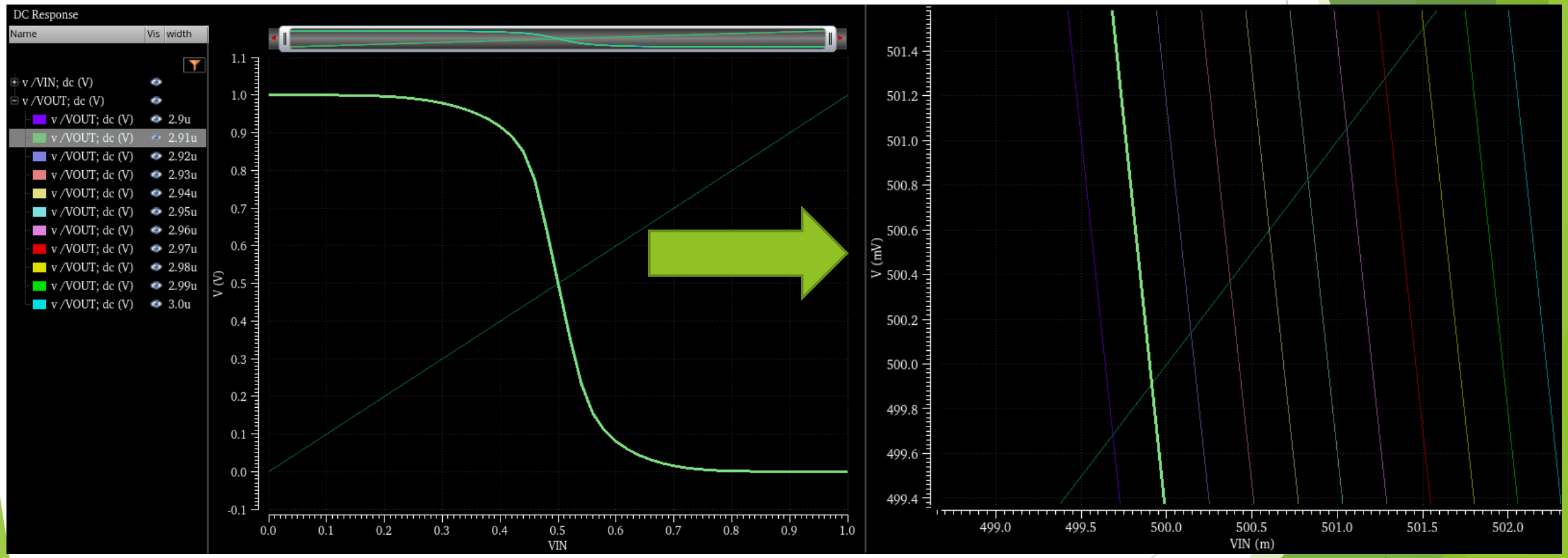
2-1. Logic Gate

Width of PMOS (NMOS W/L = 1μm/100nm , PMOS L = 100nm)



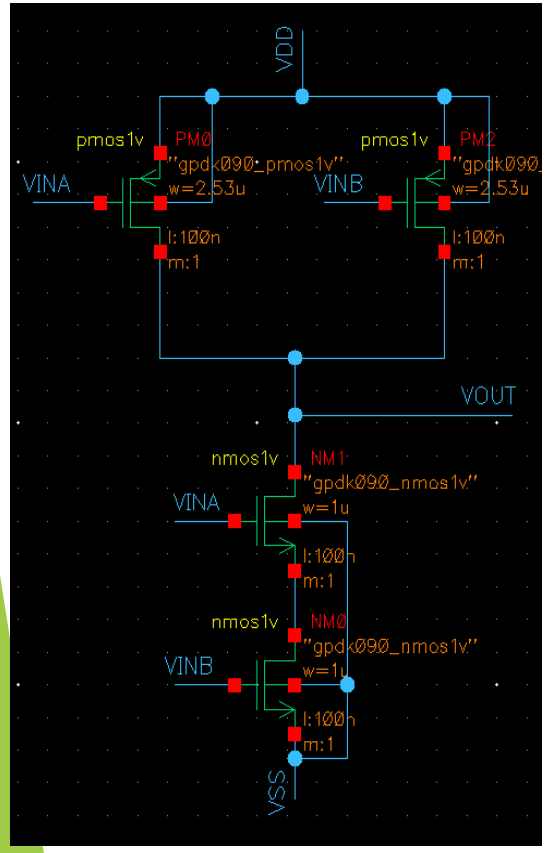


2-1. Logic Gate

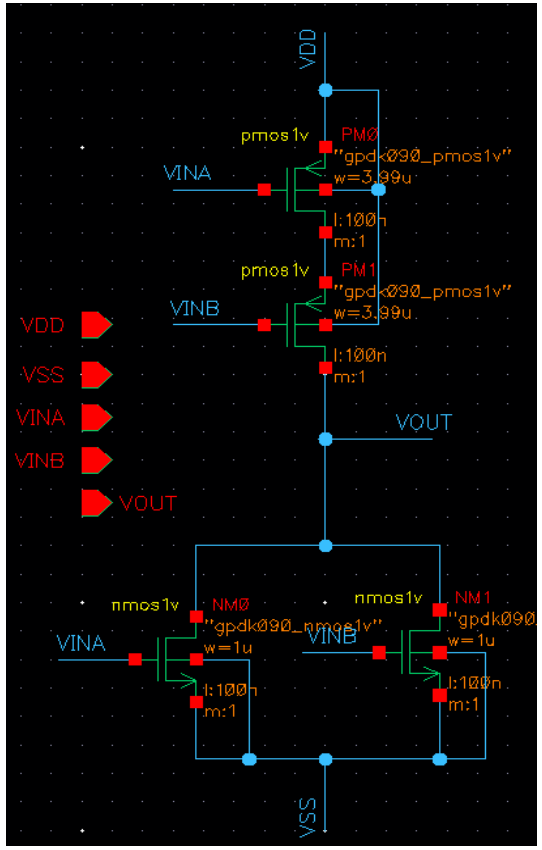


2-1. Logic Gate

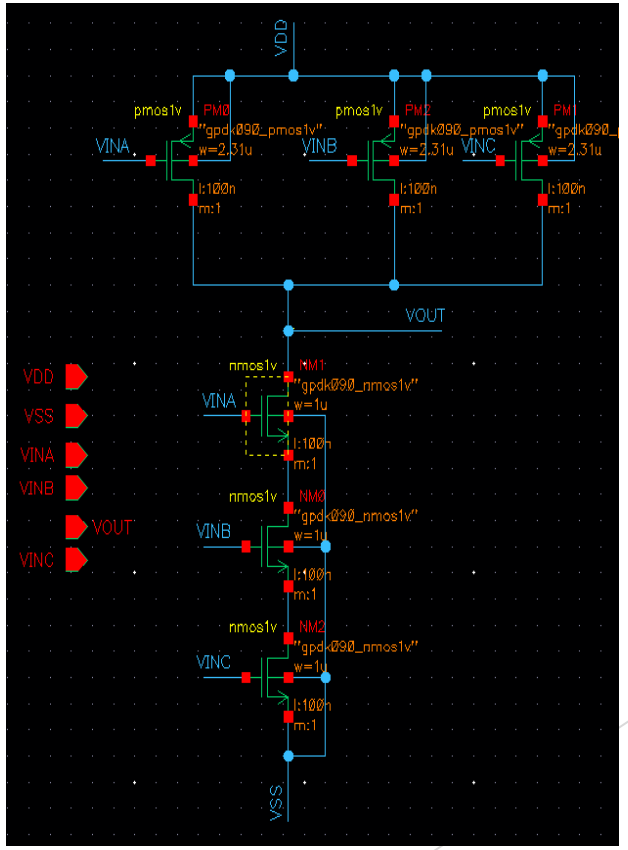
2NAND - 2.53μm



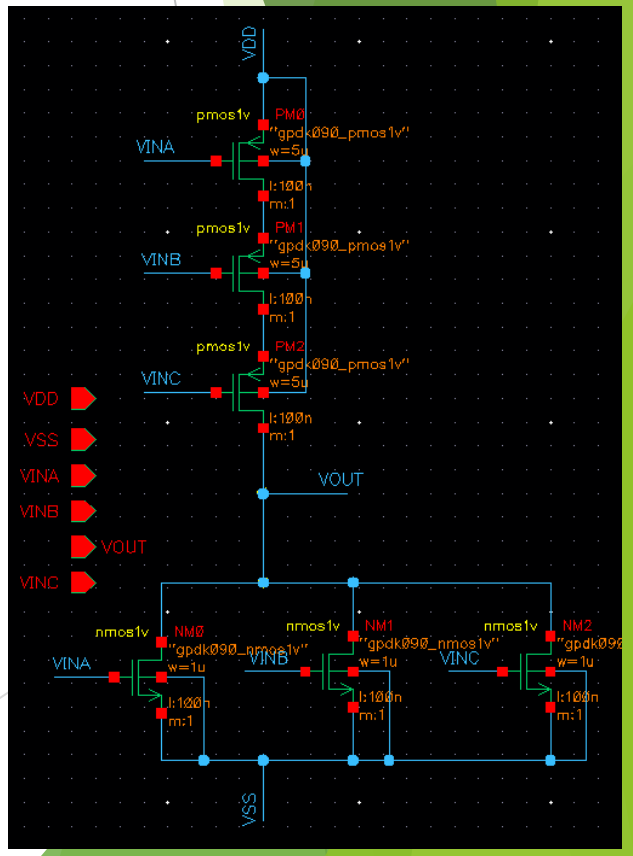
2NOR - 3.99μm



3NAND - 2.31μm

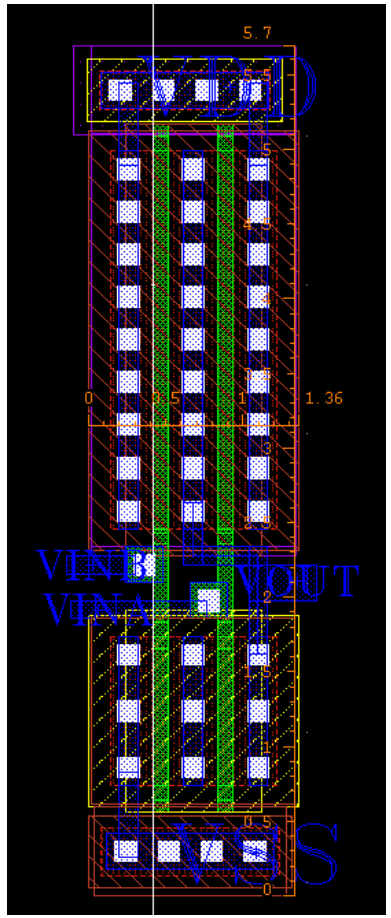


3NOR - 5μm

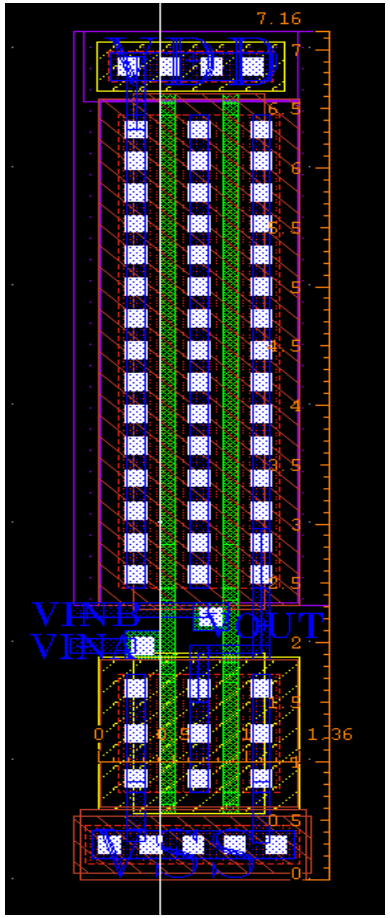


2-1. Logic Gate

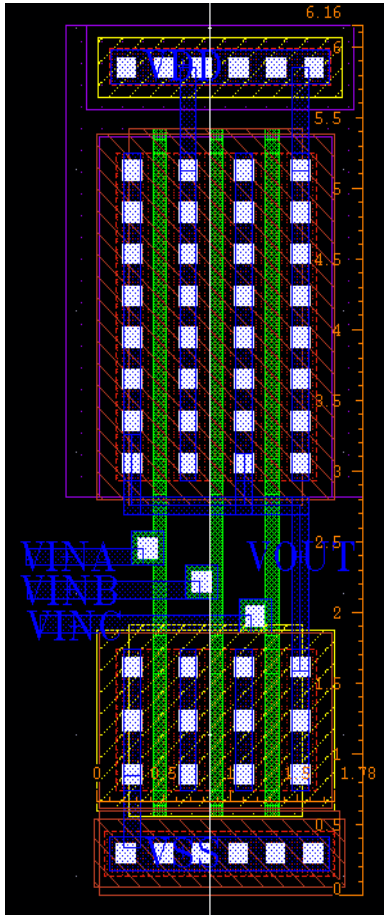
2NAND



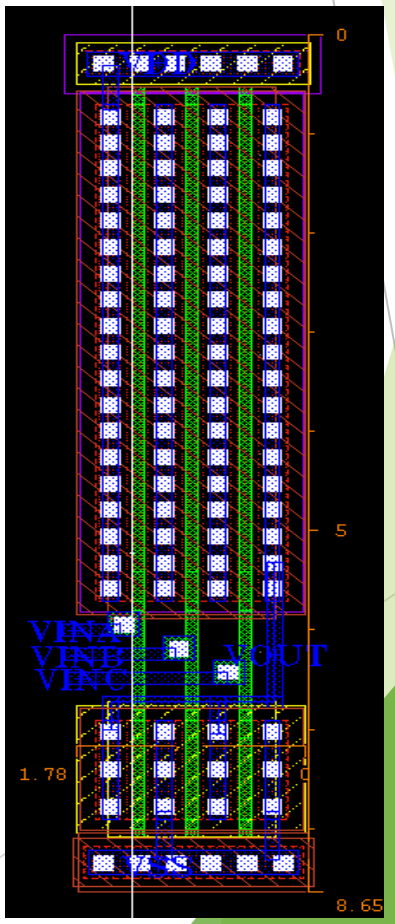
2NOR



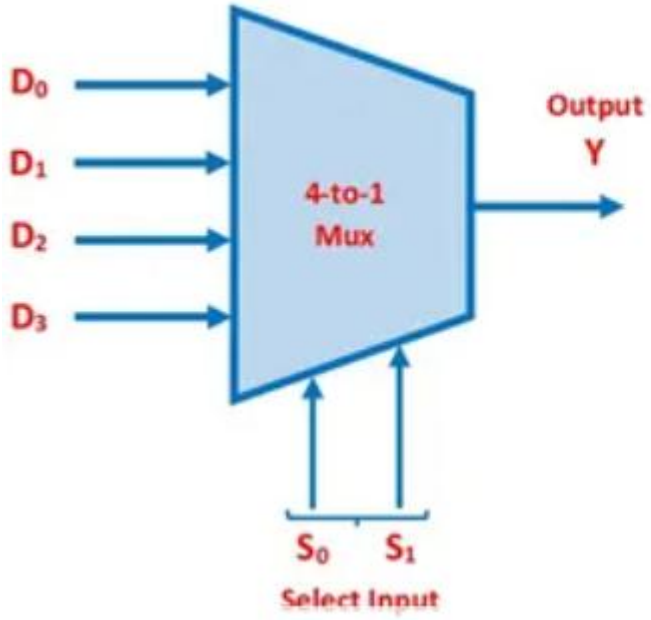
3NAND

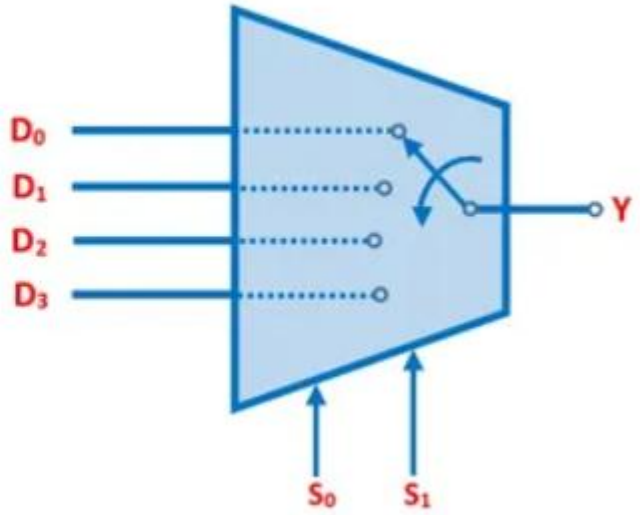


3NOR



2-2. Multiplexer (MUX)

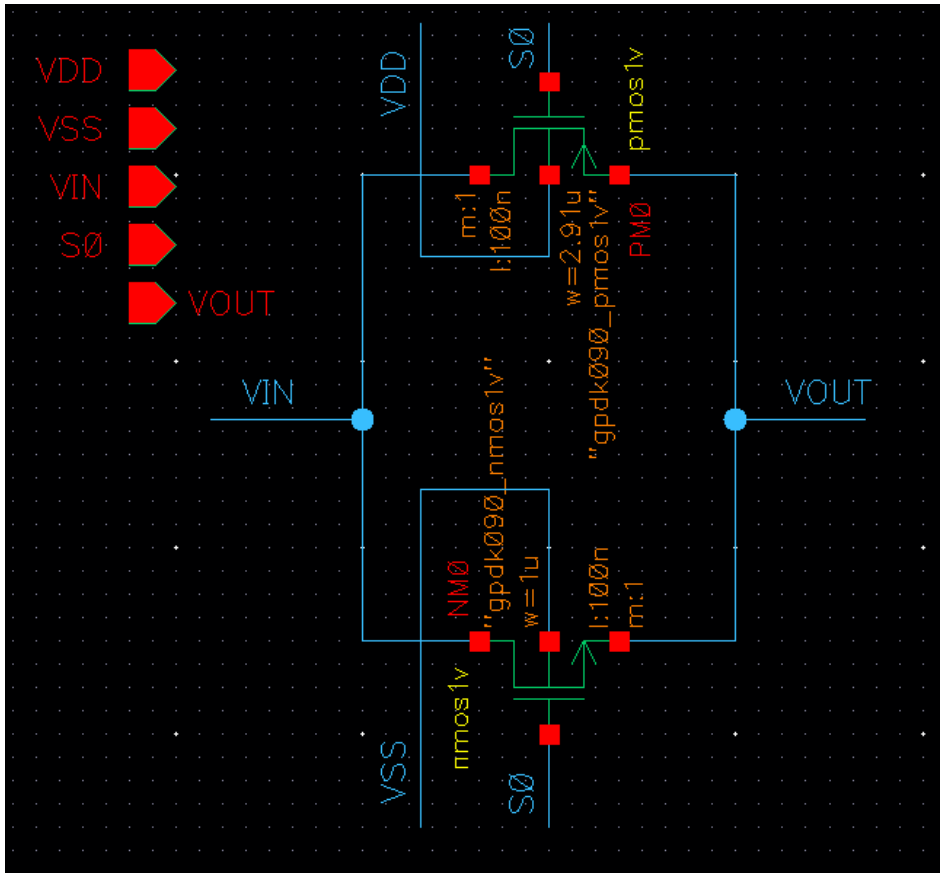


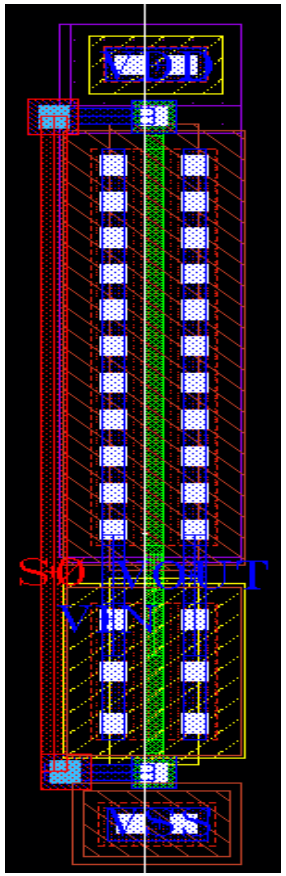


-receive multiple input signal and synthesize a single output

2-2. Multiplexer (MUX)

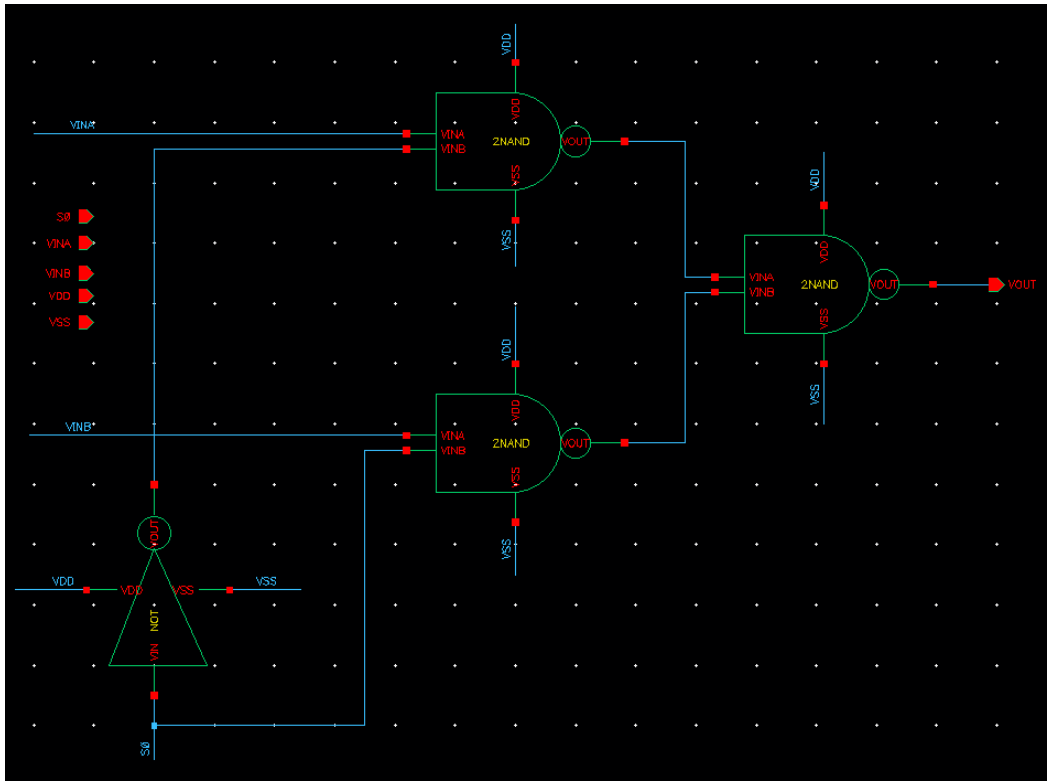
Switch (Transmission gate)



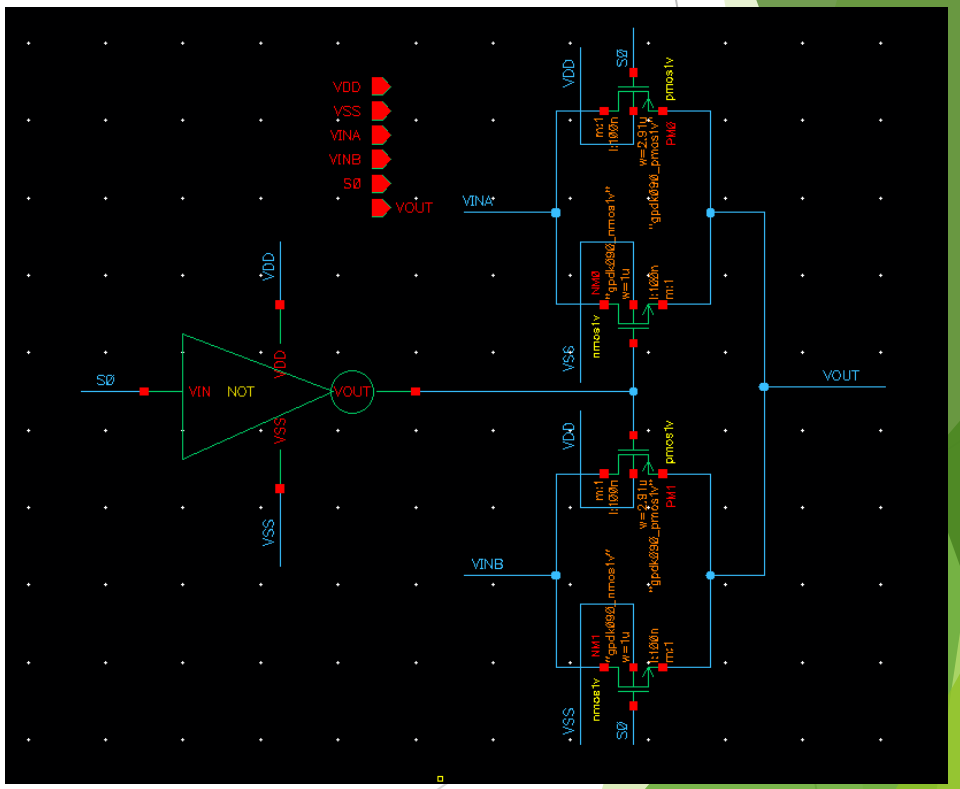


2-2. Multiplexer (MUX)

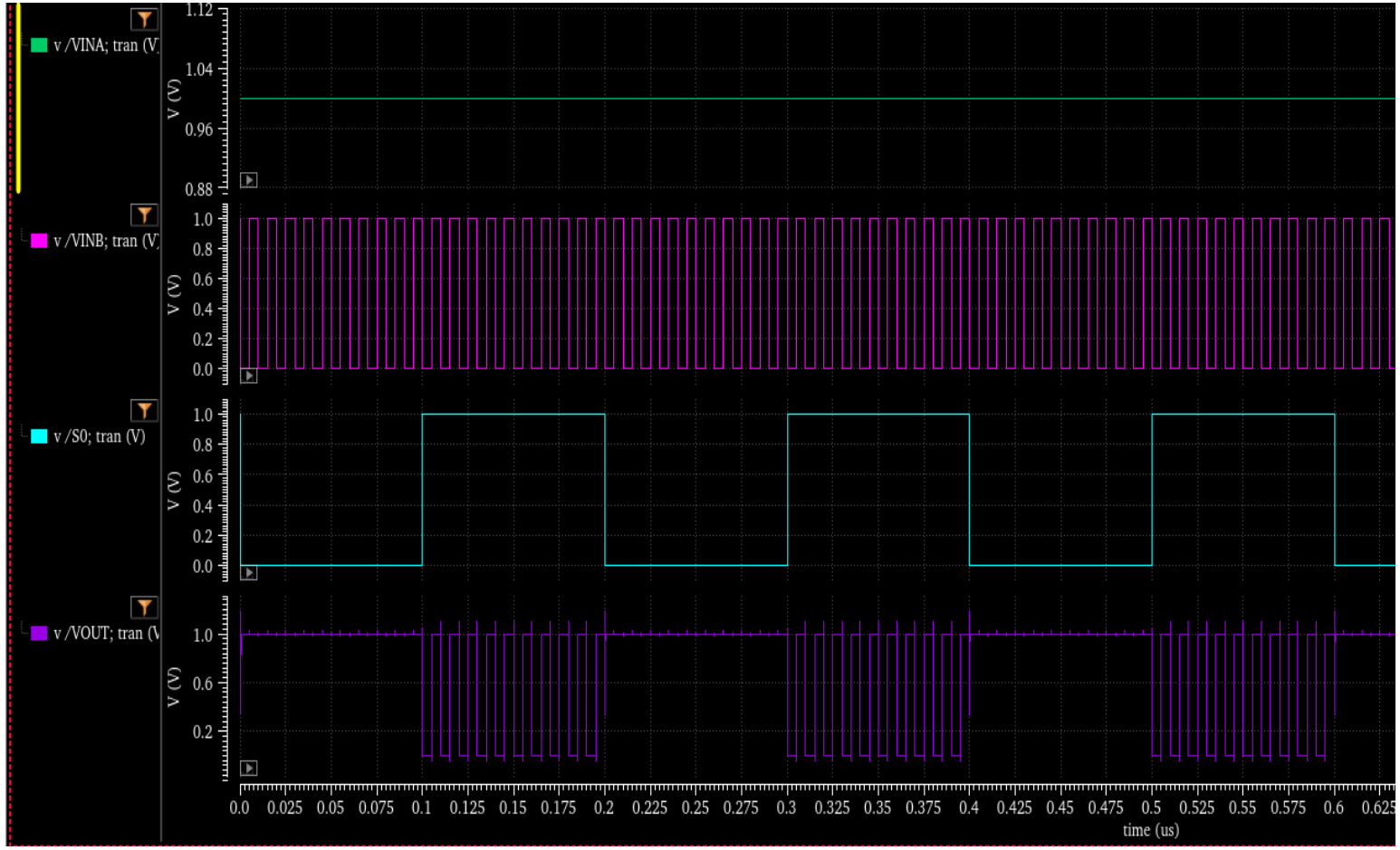
2x1 MUX (Logic Gate)



2x1 MUX (Switch)



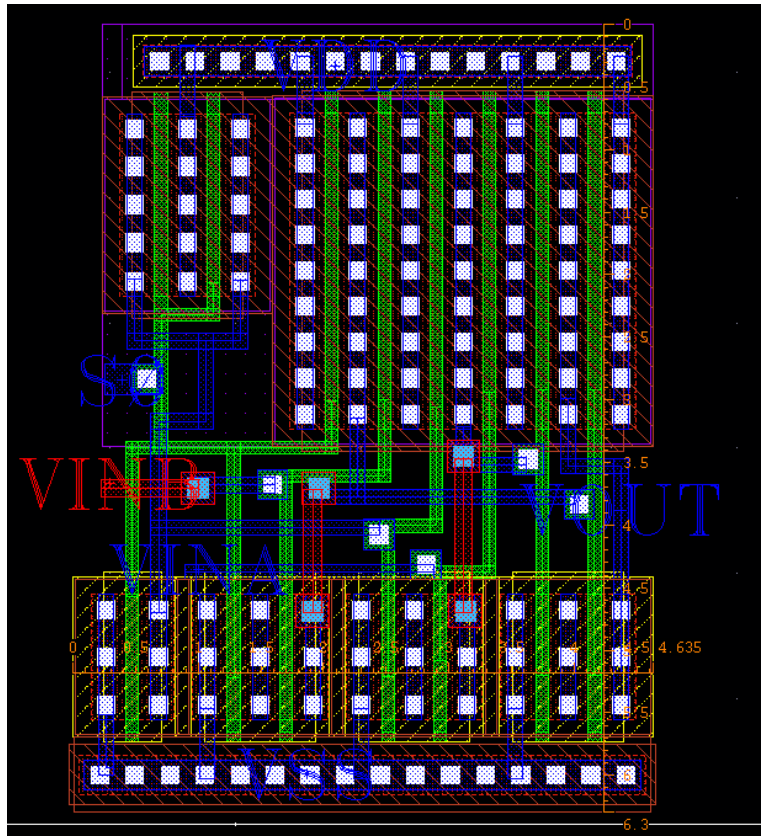
2-2. Multiplexer (MUX)



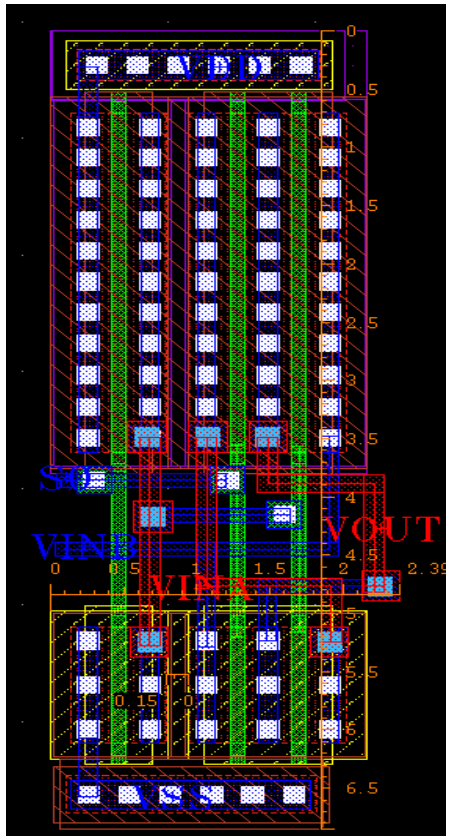
S0	VOUT
0	VINA
1	VINB

2-2. Multiplexer (MUX)

2x1 MUX (Logic Gate)



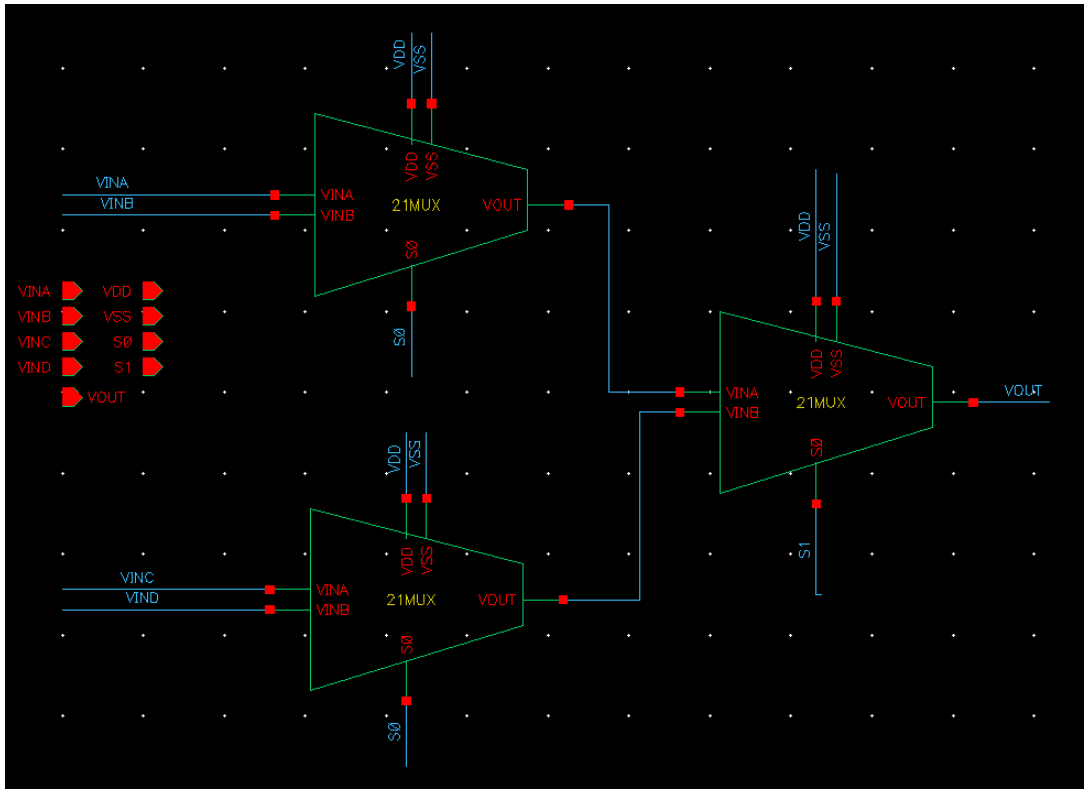
2x1 MUX (Switch)



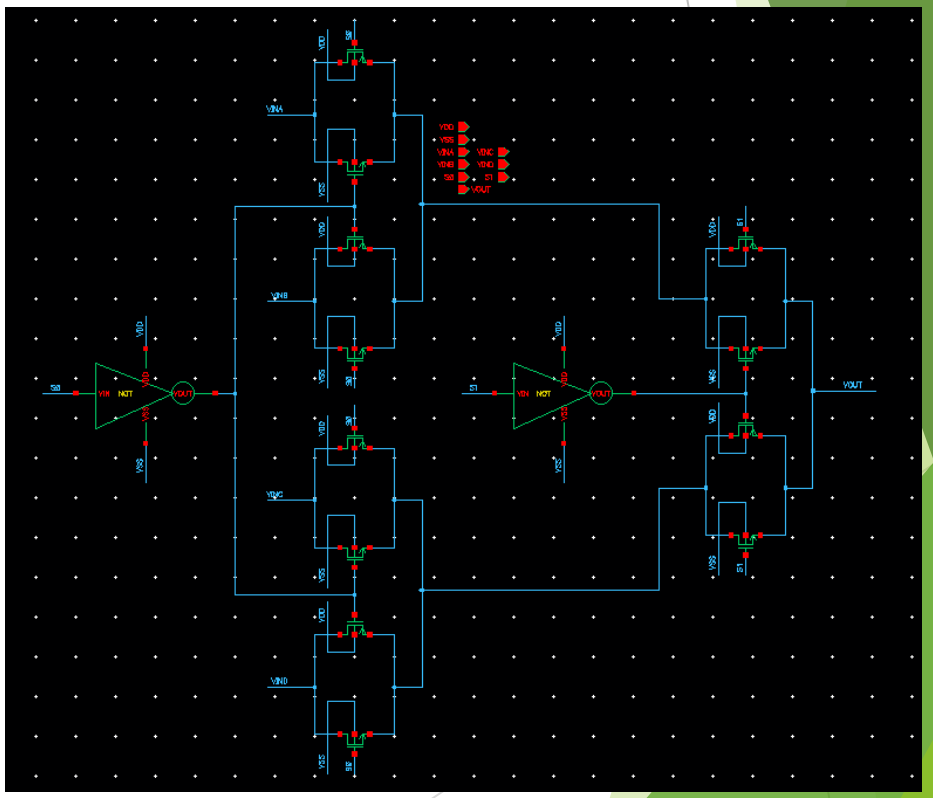
	Logic	Switch
Width	4.635	2.39
Length	6.3	6.86
Area	29.2	16.4
TR	14	6

2-2. Multiplexer (MUX)

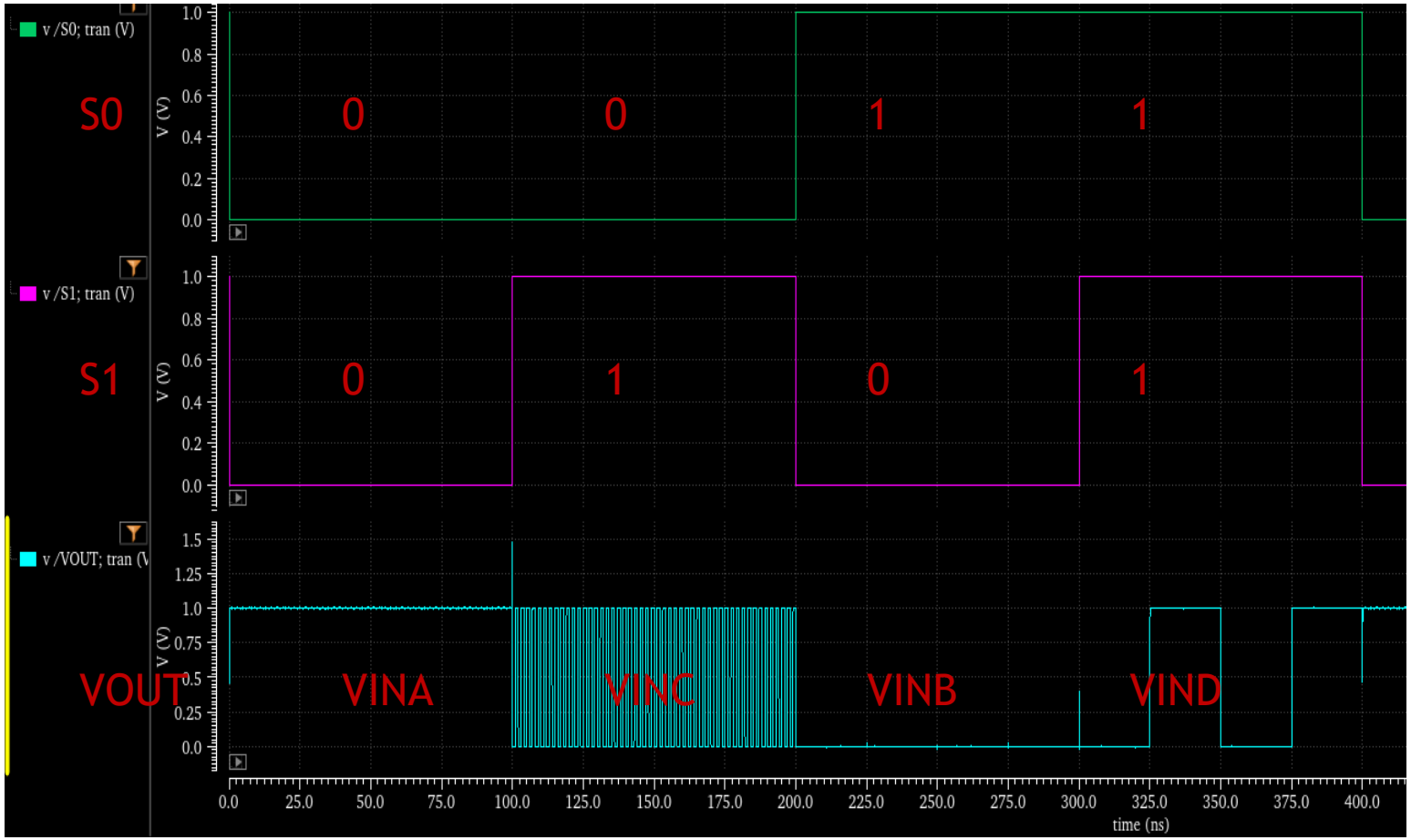
4x1 MUX (Logic Gate)

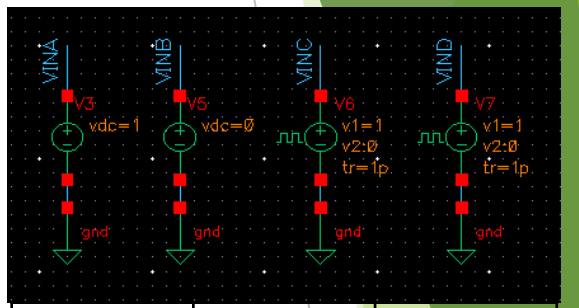


4x1 MUX (Switch)



2-2. Multiplexer (MUX)

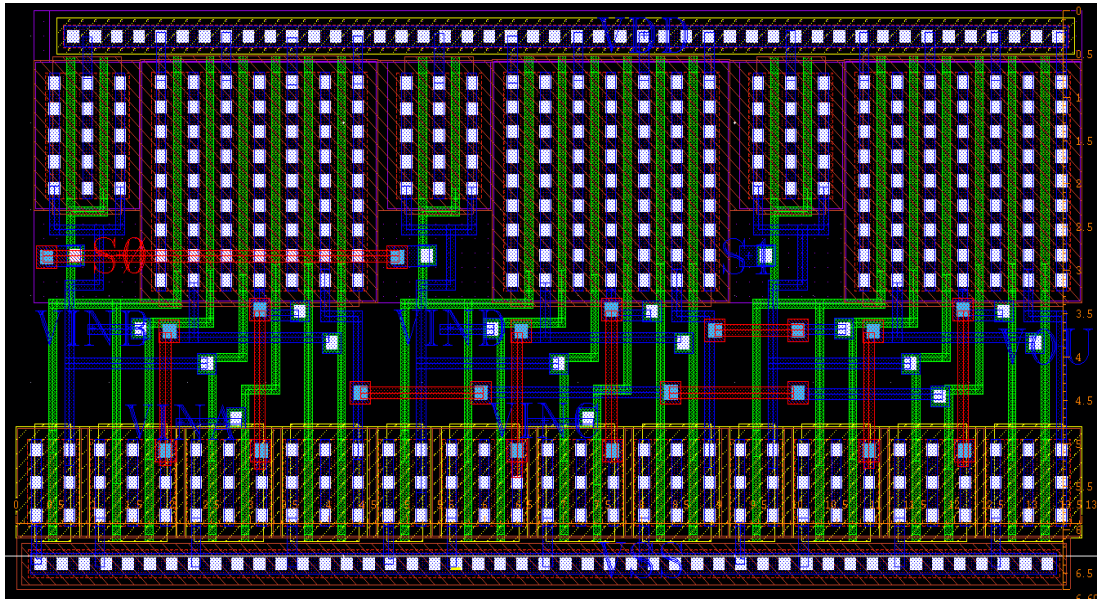




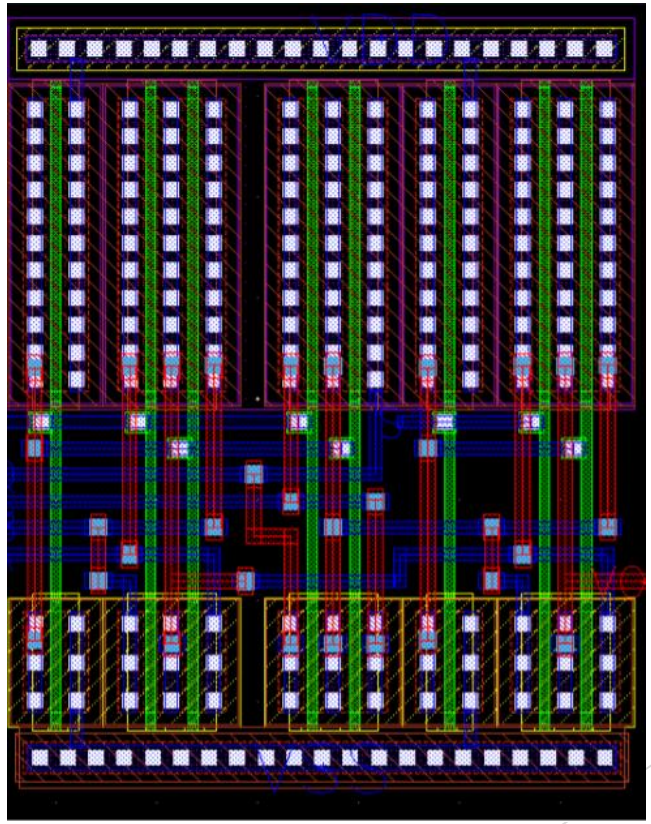
S1	S0	VOUT
0	0	VINA
0	1	VINB
1	0	VINC
1	1	VIND

2-2. Multiplexer (MUX)

4x1 MUX (Logic Gate)



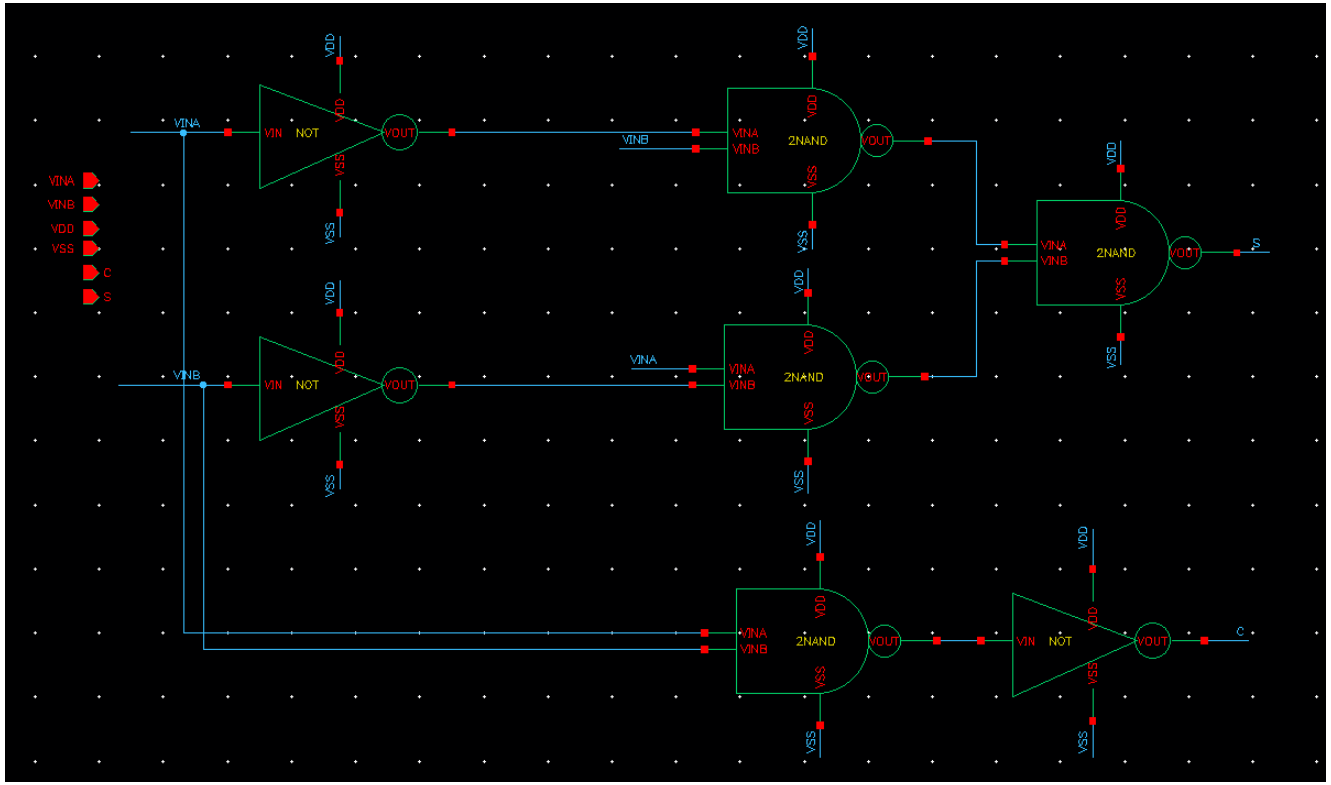
4x1 MUX (Switch)



	Logic	Switch
Width	13.635	6.01
Length	6.695	6.94
Area	91.286	41.709
TR	42	16

2-3. Adder

Half Adder

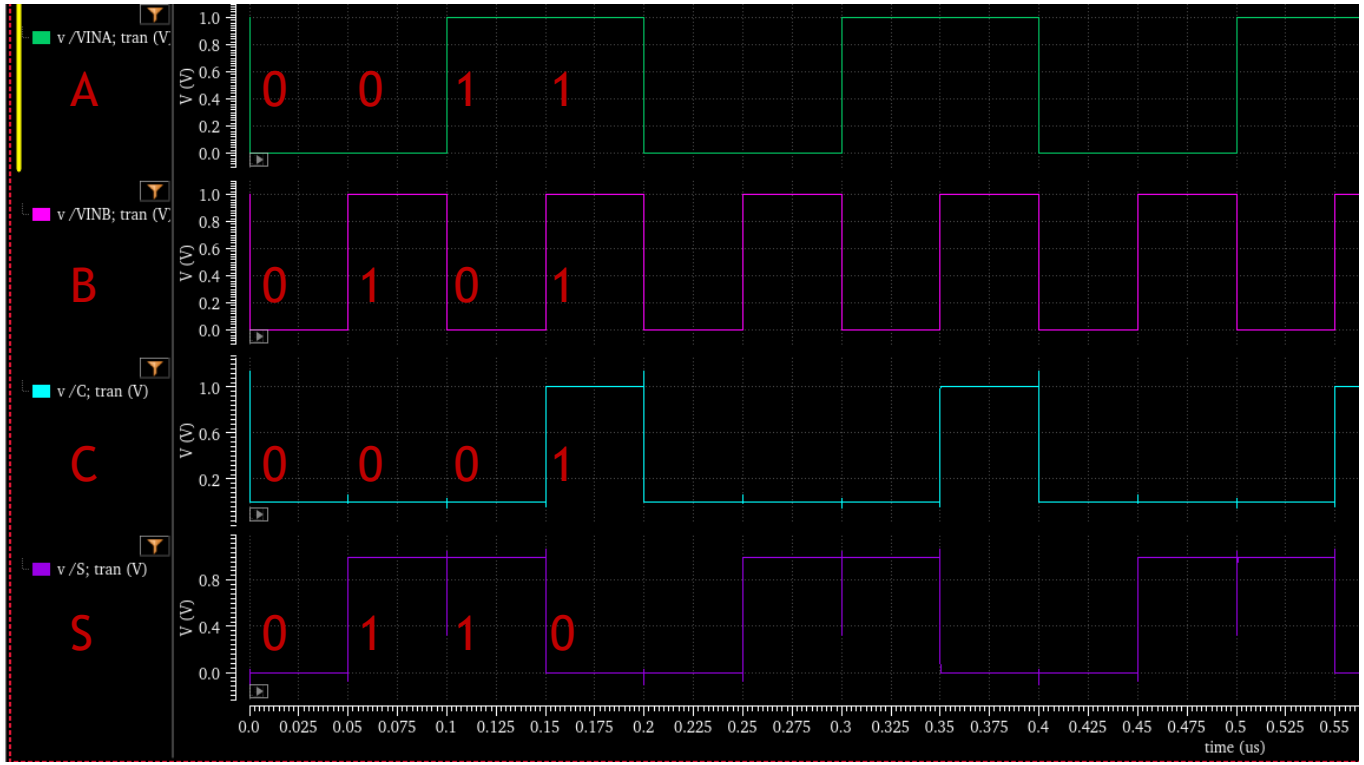


C = AB
S = A'B + B'A

A	B	C	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

2-3. Adder

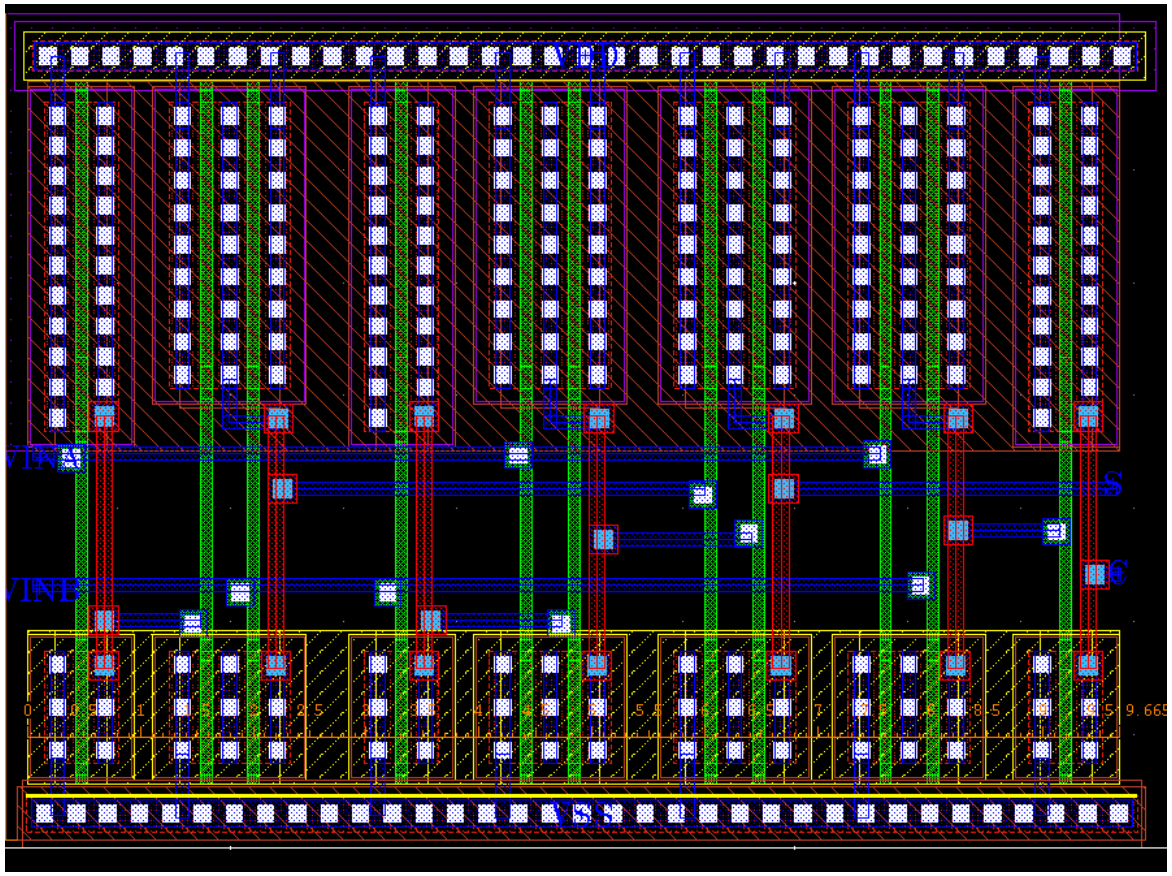
Half Adder



A	B	C	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

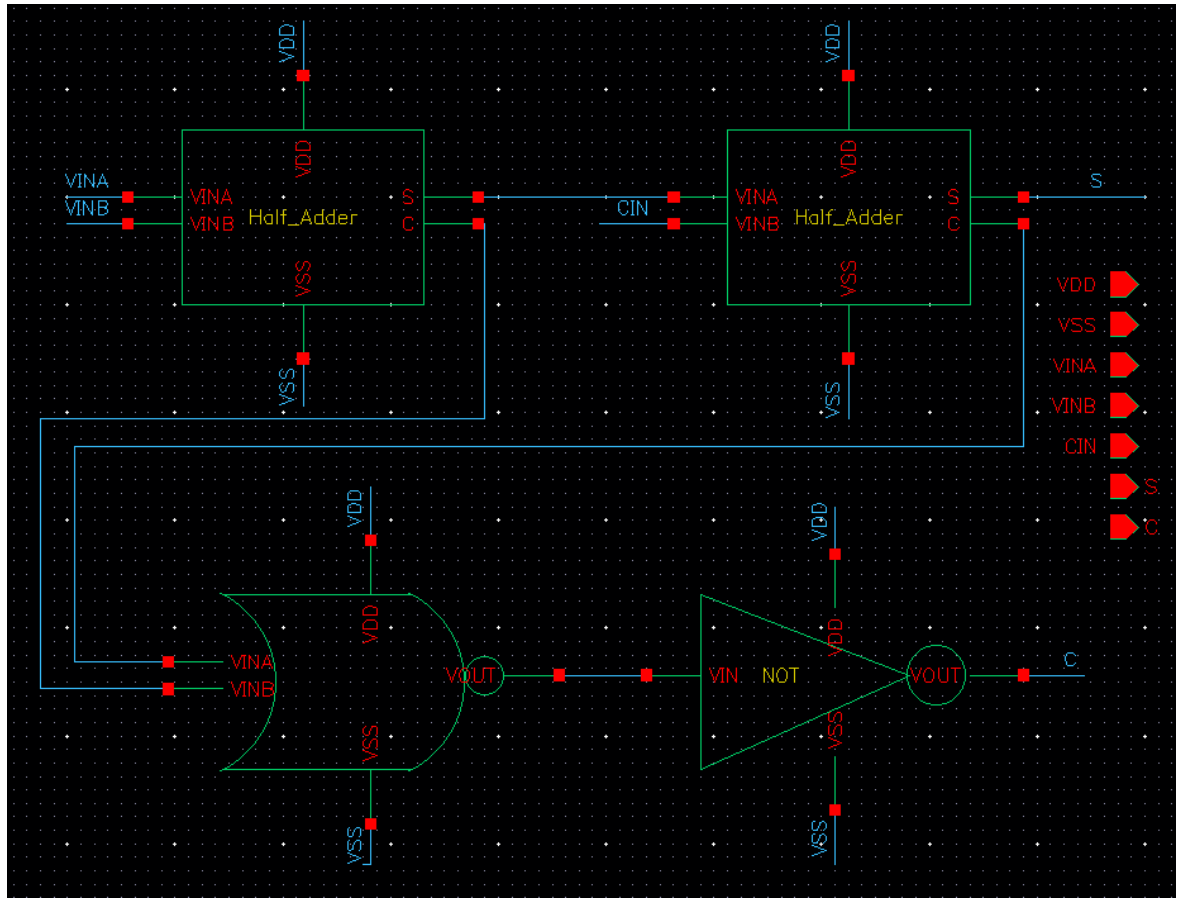
2-3. Adder

Half Adder



2-3. Adder

Full Adder



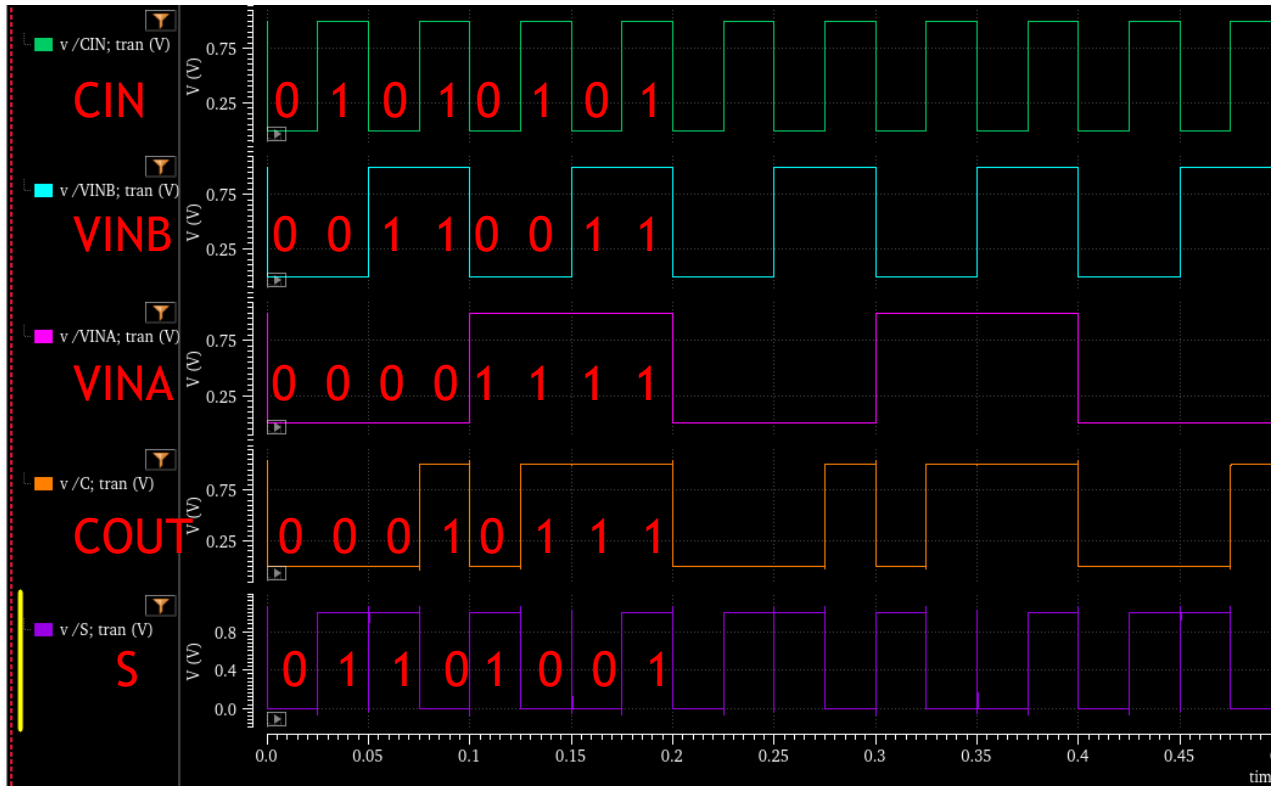
COUT = ABC + A'BC + AB'C + ABC'

S = ABC + A'B'C + A'BC' + AB'C'

A	B	CIN	COUT	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

2-3. Adder

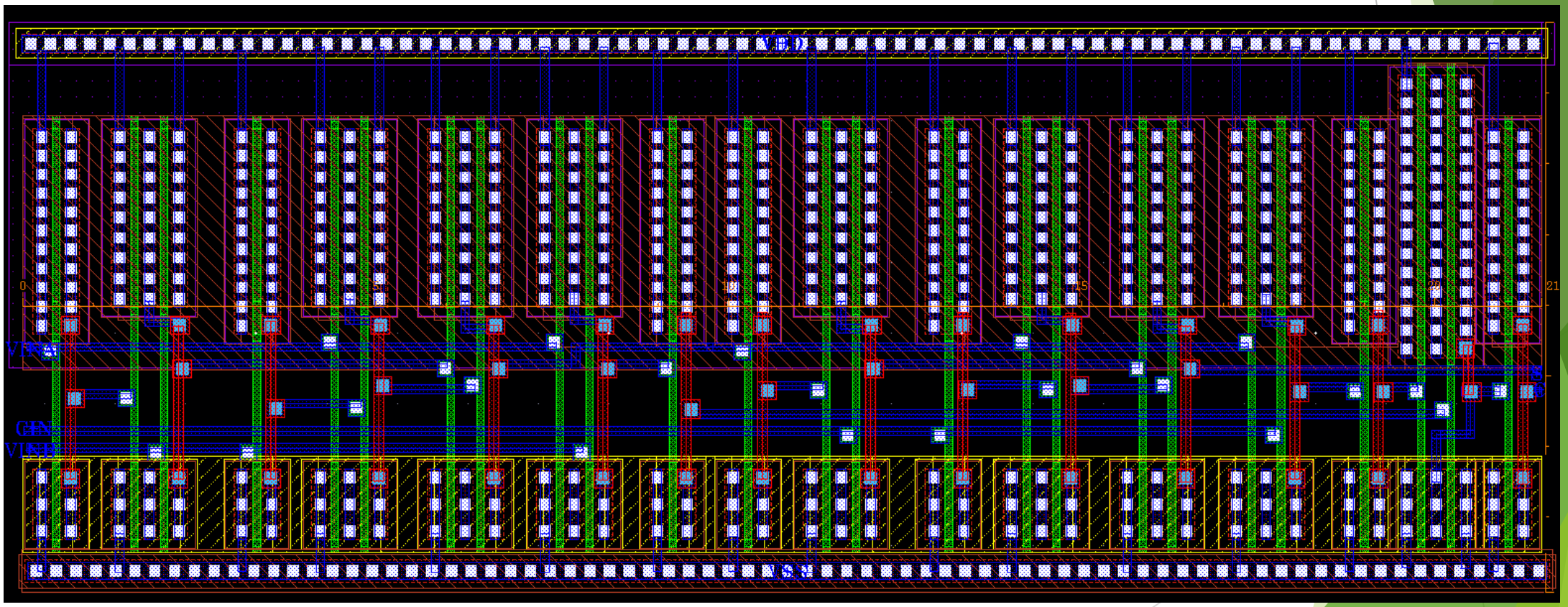
Full Adder



A	B	CIN	COUT	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

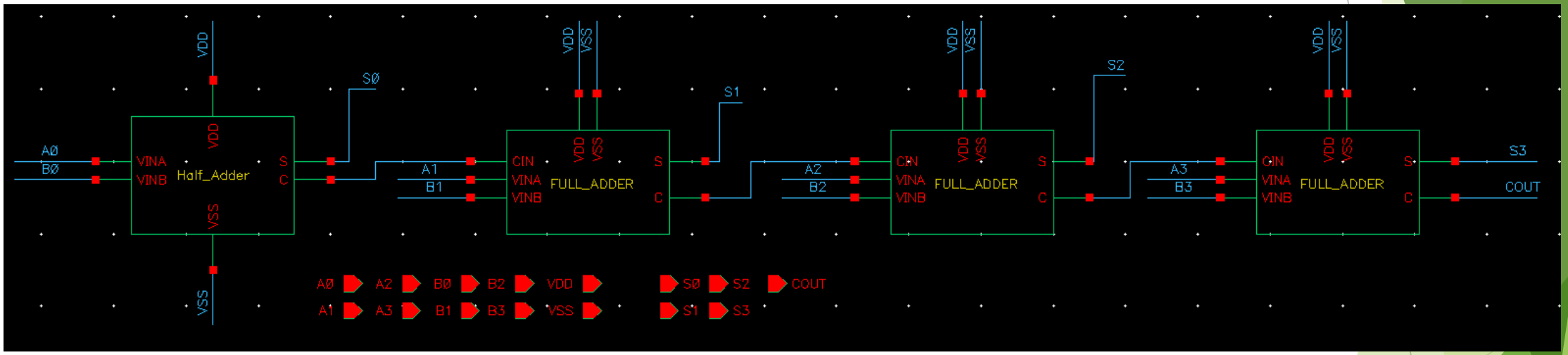
2-3. Adder

Full Adder



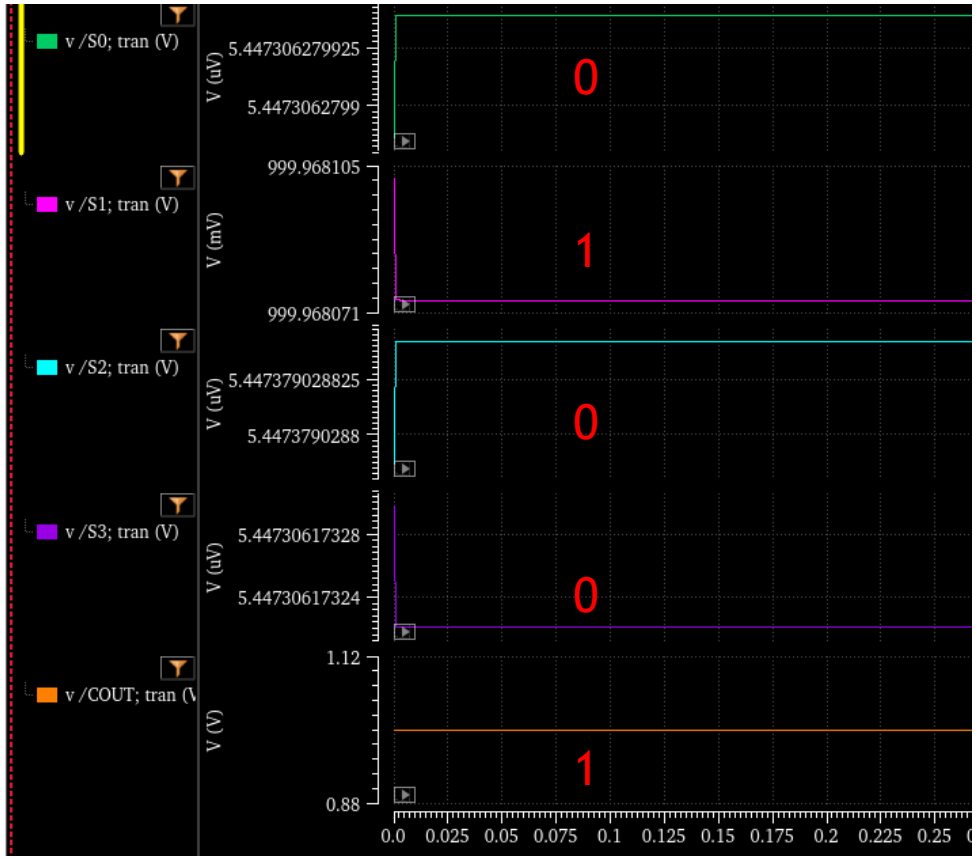
2-3. Adder

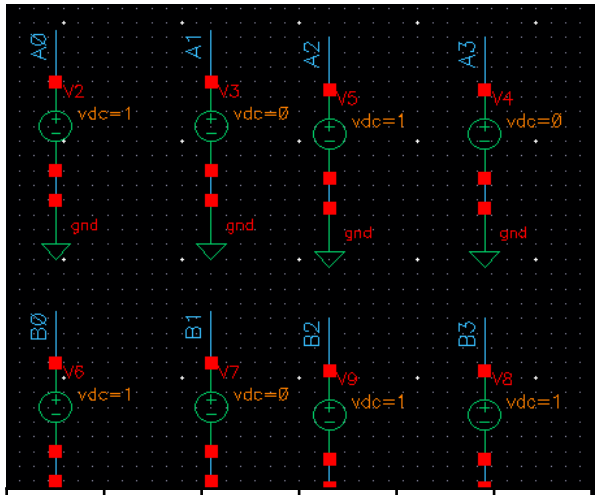
4-bit Adder



2-3. Adder

4-bit Adder

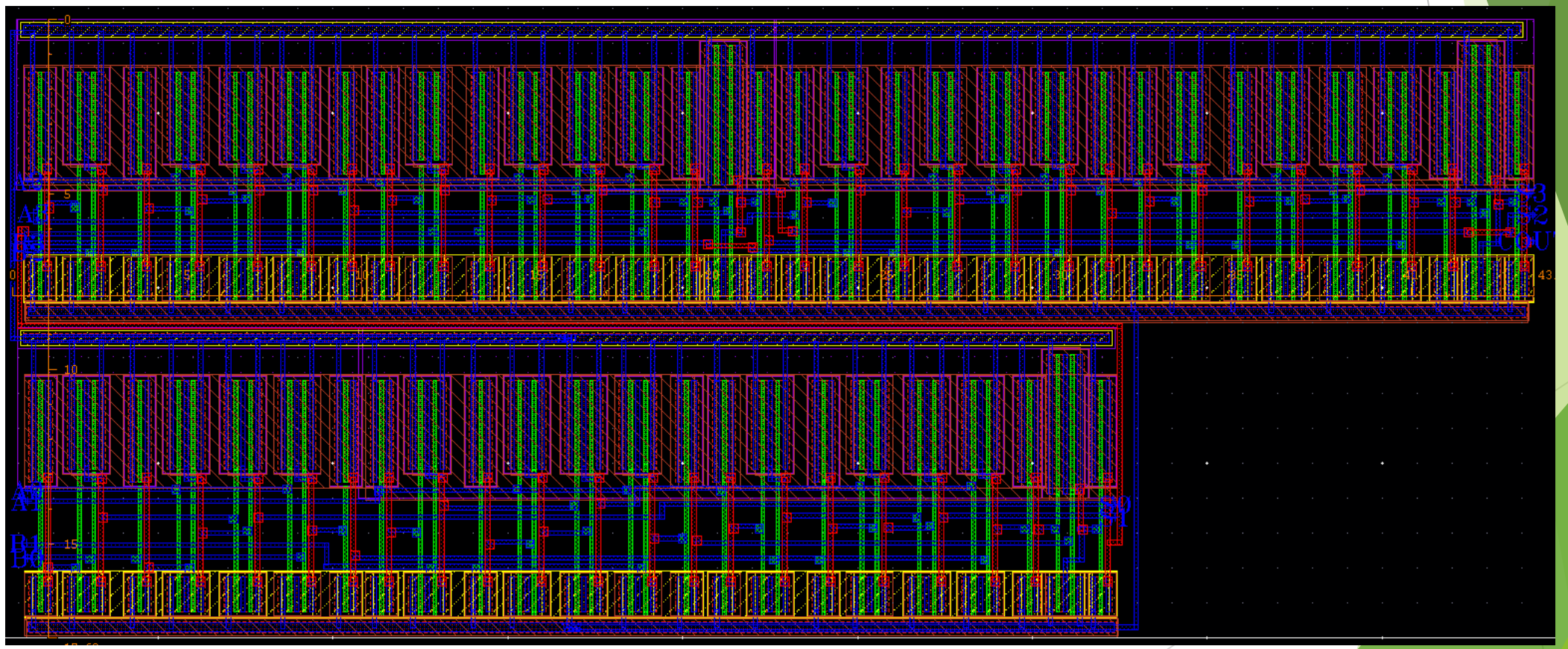




	C	3	2	1	0
A		0	1	0	1
B		1	1	0	1
S	1	0	0	1	0

2-3. Adder

4-bit Adder

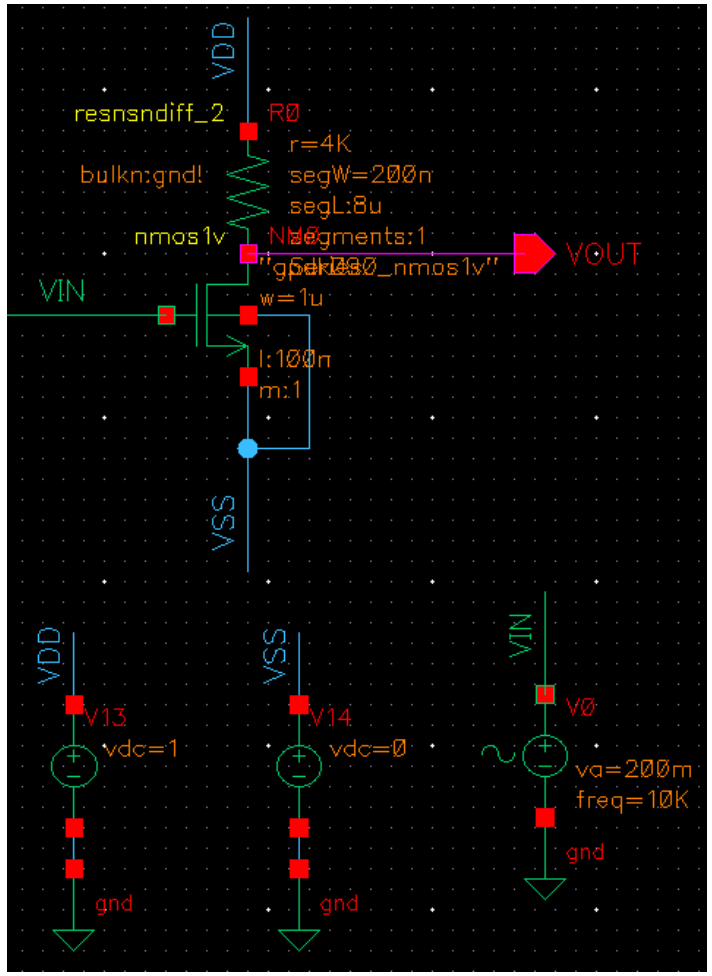


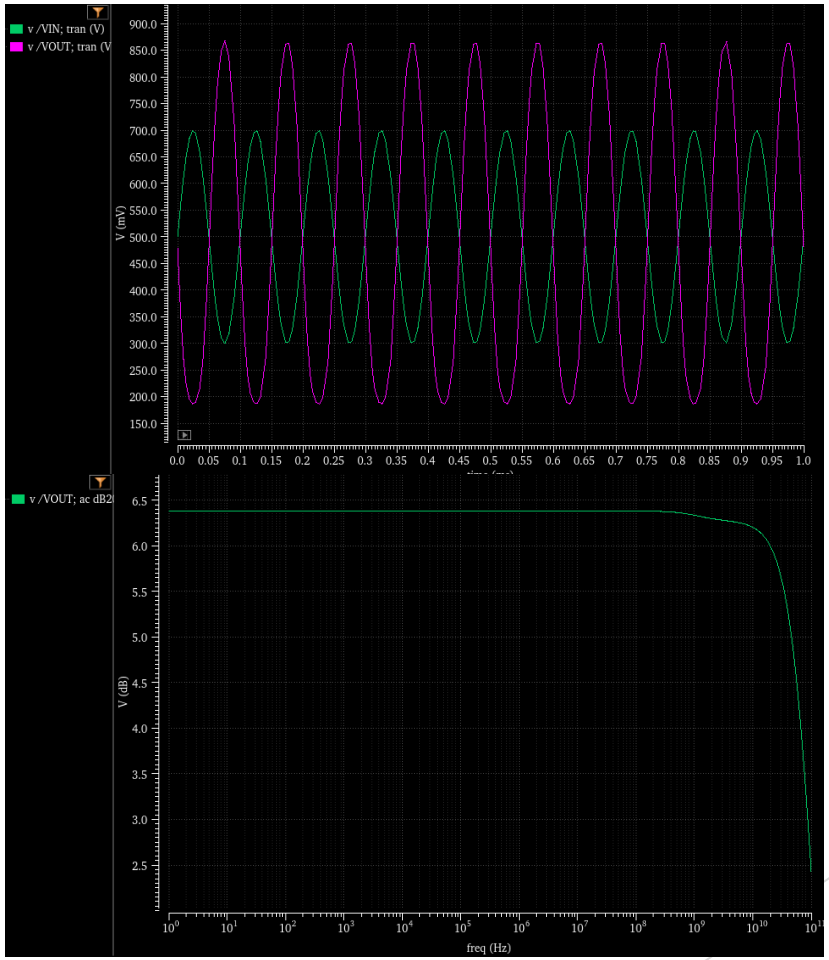
3. Analog Circuit

- Common Source Amplifier

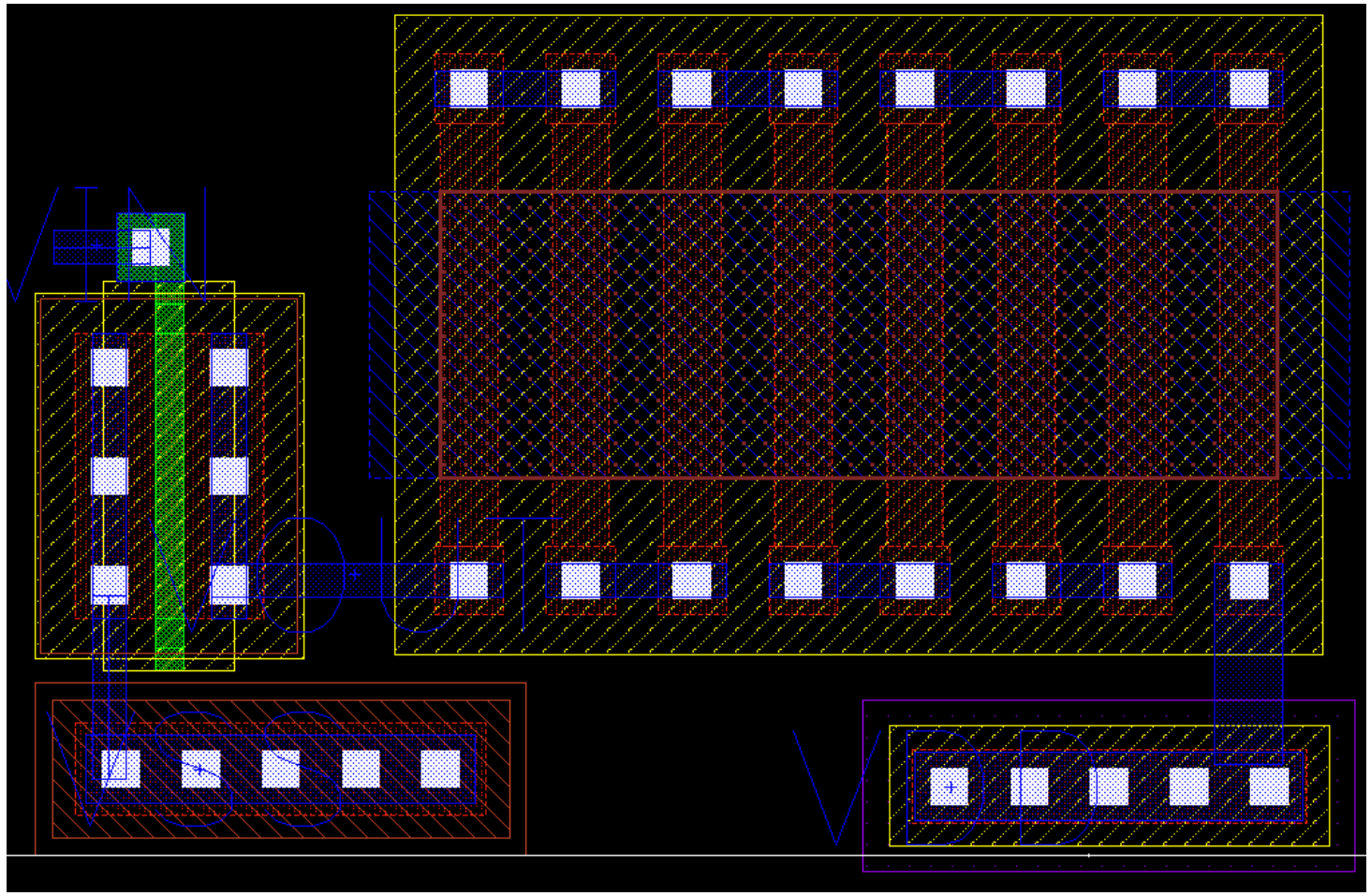
- Differential Amplifier

3-1. CS Amplifier

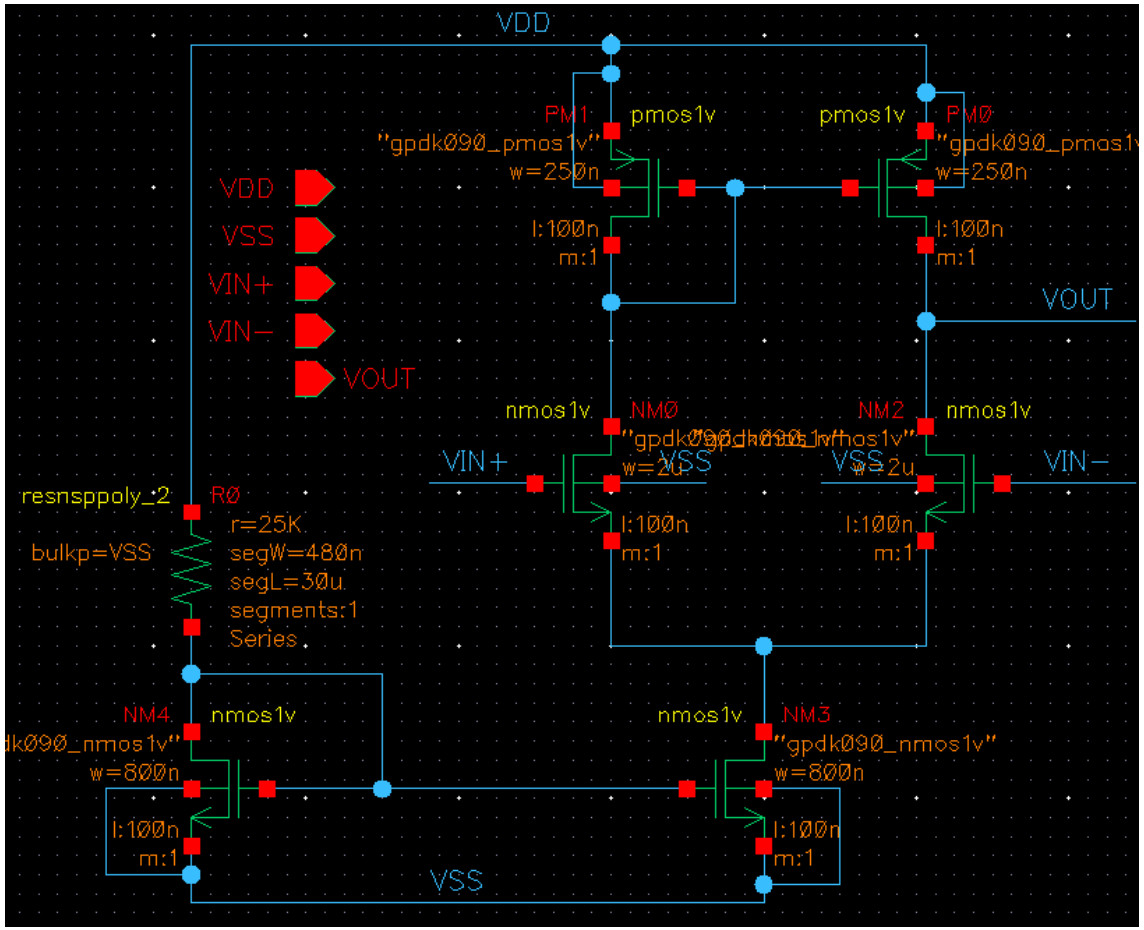


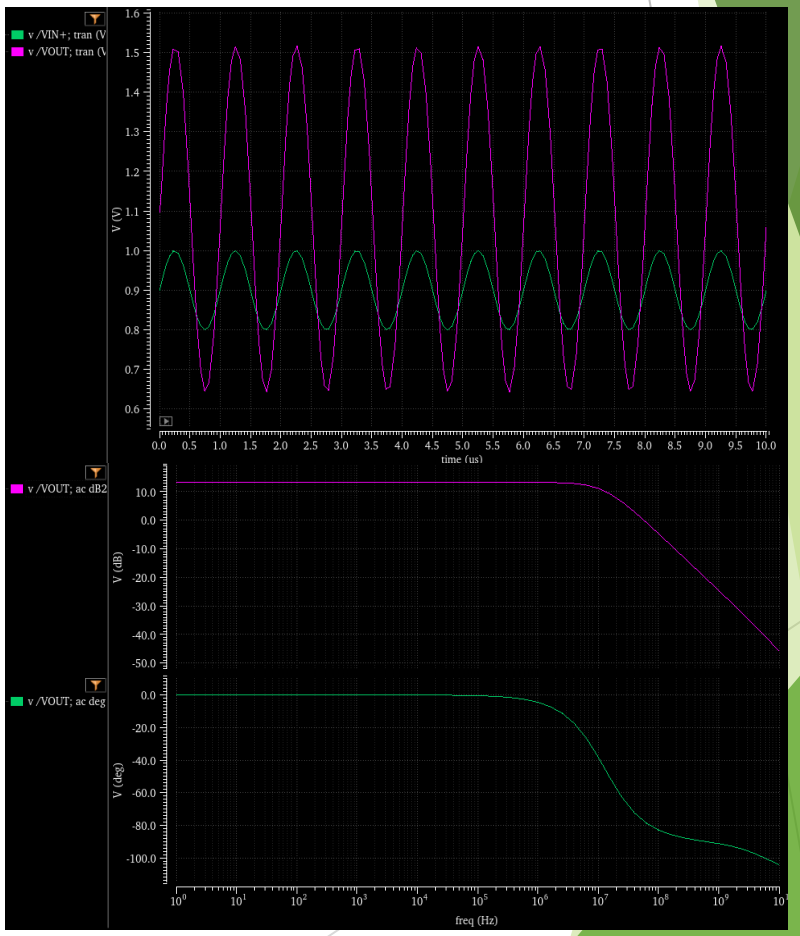


3-1. CS Amplifier



3-2. Differential Amplifier





3-2. Differential Amplifier